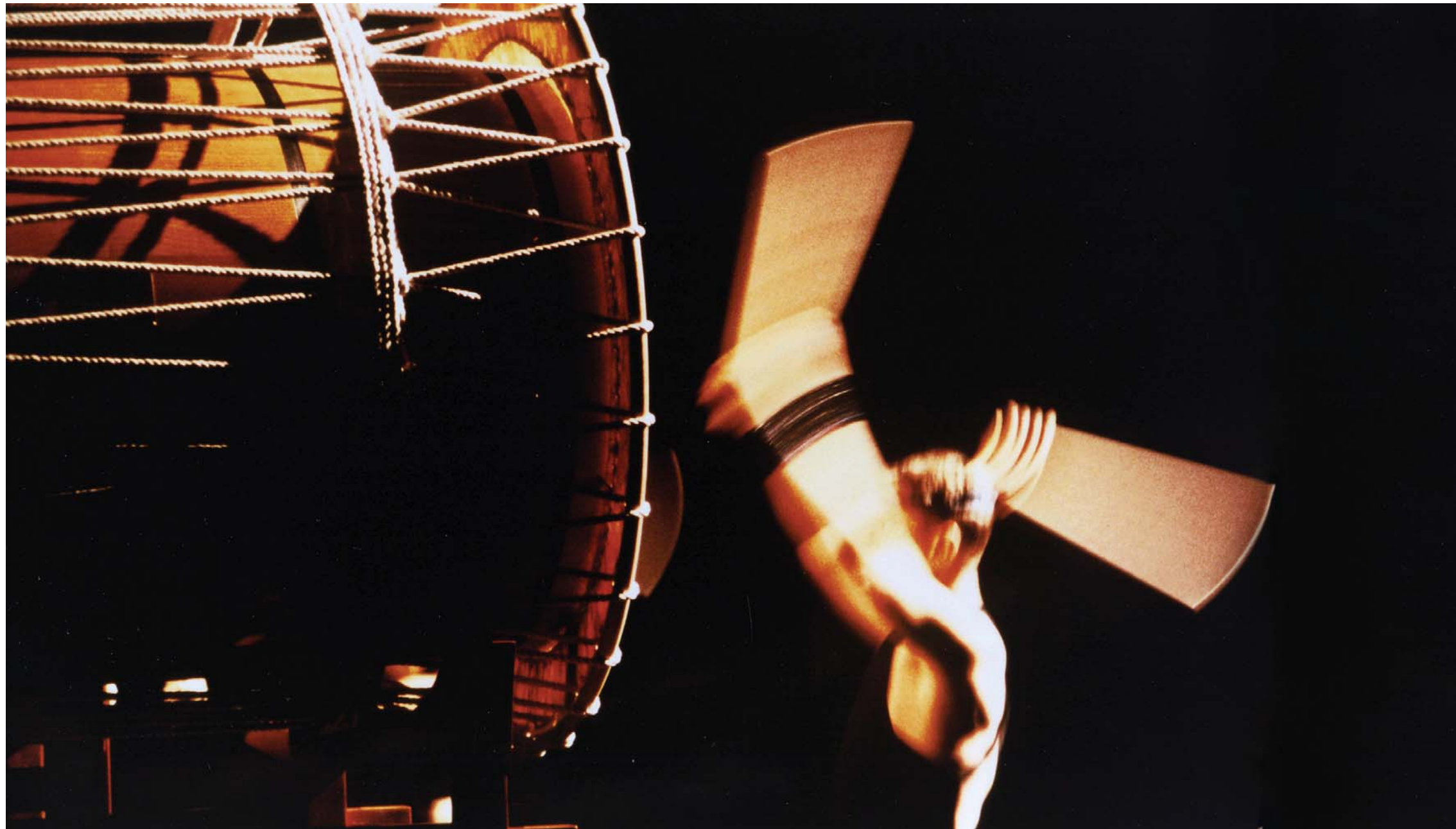


'When they assemble the chip to include the digital and analogue sections, it starts to demonstrate strange behaviours'

**Mentor Graphics'**  
Hazem Hegazy is putting together a PhD that deals with ways of speeding up the simulation of cross-chip noise and its impact on analogue and RF blocks.



Portland Talko

# noise annoys

Digital and analogue circuits have never been that happy together. The noise pollution from logic circuits hammering away is only going to get worse. By **Chris Edwards**

For designers of system-on-chip (SoC) devices, the next frontier in terms of integration lies in the analogue domain. The design teams are now looking to pull together hundreds of cores from various sources. Many are digital, but the demand to put analogue cores on-chip is growing. But the high clock-speed SoC is a hostile environment for these cores.

Sandy Mehndiratta, product

marketing director for Cadence's simulation tools in the Virtuoso group, said: "People are getting more aggravated cross-chip noise effects. We are definitely seeing a trend from our customer base and it is an area we are investigating."

Francois Clement, chief technology officer at French startup Coupling Wave Solutions, said the issue of noise is becoming more problematic as

designers are adding circuits that act as strong noise sources, such as power management units (PMU).

"The addition of the PMU is becoming a nightmare. It is becoming a significant generator of noise," said Clement.

Worse, they may be forced to use substrates that are more highly doped to get acceptable performance out of deep submicron processes, Clement claimed. The higher doping leads to lower impedance and can render guard rings almost useless in some cases.

## SUBSTRATE CHANGES

Hazem Hegazy, a Mentor Graphics marketing engineer who is currently preparing a PhD on noise coupling at the University of Cairo, said the picture on substrate doping varies widely. "The more advanced processes tend to get more highly doped but that is not always the case. The IDMs can control their doping. They can ask for increased doping to provide better protection against lock-up. So the higher doping levels can be in older technologies."

As the environment may be getting noisier around the blocks, Clement added: "On the other side, the specifications of the more advanced radios are getting tighter and more difficult to reach." He said the tighter specifications mean that the 20dB saving you can expect from a guard ring may not be enough without a more radical redesign of some of the cores or the use of a different package.

"The combination of the feature size, the number of devices that can be put on the silicon and the features that the silicon integrators want to provide is now pushing people to put more analogue circuitry on the same silicon."

Clement claimed some teams are being tripped up by noise issues as they put the final touches on their large, multi-million transistor systems on chip (SoCs). He said they know it is noise at the heart of the problem because early test ▶

## problems

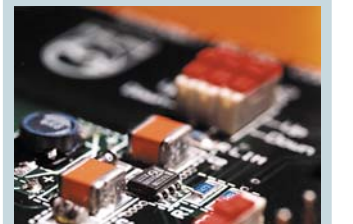
### SOURCES OF NOISE

Substrate noise gets a lot of attention but it is far from being the only source of interference for analogue blocks.

Brieuc Turluche, CEO of Coupling Wave Solutions (CWS), said the commercial noise analysis tools that exist today – such as Cadence Design Systems' SubstrateStorm, which was developed by CWS cofounder Francois Clement – tackle individual sources of noise. "None of them handle the whole chip," Turluche claimed, which includes noise coupled through the substrate, the interconnect and the package.

"We have multiple sources of substrate noise," explained Hazem Hegazy, of Mentor Graphics. "There is inductive noise: the current mainly coming from the bond wires and from the packaging as well as the long power lines in an IC."

Noise can be coupled through the interconnect lines of a chip,



said Francois Clement. With the arrival of switching power converters on-chip, designed to provide blocks inside with individually set voltage levels, more noise is being coupled through the power grid and interconnect.

Impact ionisation in high-speed, deep submicron transistors is a further source of noise that can be coupled through the substrate. But, Hegazy explained: "The dominant source is ground and supply bounce on the power rails. This is about 98 per cent of the amount of the noise source. There is some impact on digital circuits from this. But the analogue design is the most vulnerable."

Clement said external noise sources are becoming more important: "We see that coming and now we are working on a specific development to address this."

'You can't expect guard rings to get rid of the noise completely, and a guard ring may need an expensive package. If designed correctly, you win a maximum of 10 to 20dB attenuation.'

Electromagnetic interference gets everywhere and the substrates used in modern chips are making life worse. So, companies such as Coupling Wave Solutions are coming up with tools (bottom right) that can at least point out potential trouble spots for analogue circuits.

◀ chips that may include just a simple receiver stage or a transceiver work, but that the circuits fail in the final SoC. "When they assemble the chip to include the digital and analogue sections, it starts to demonstrate strange behaviours."

Clement said teams want to know earlier whether it is possible to build some of the more ambitious projects – that noise will not render them unusable. So, there is a growing demand for modelling techniques to give designers a much better idea of what the noise will be like much earlier in the design process.

Today, many designers use custom techniques for estimating how much noise will be coupled through the substrate, for example, from digital cores to analogue circuits. Plugged into simulation tools such as Cadence Design

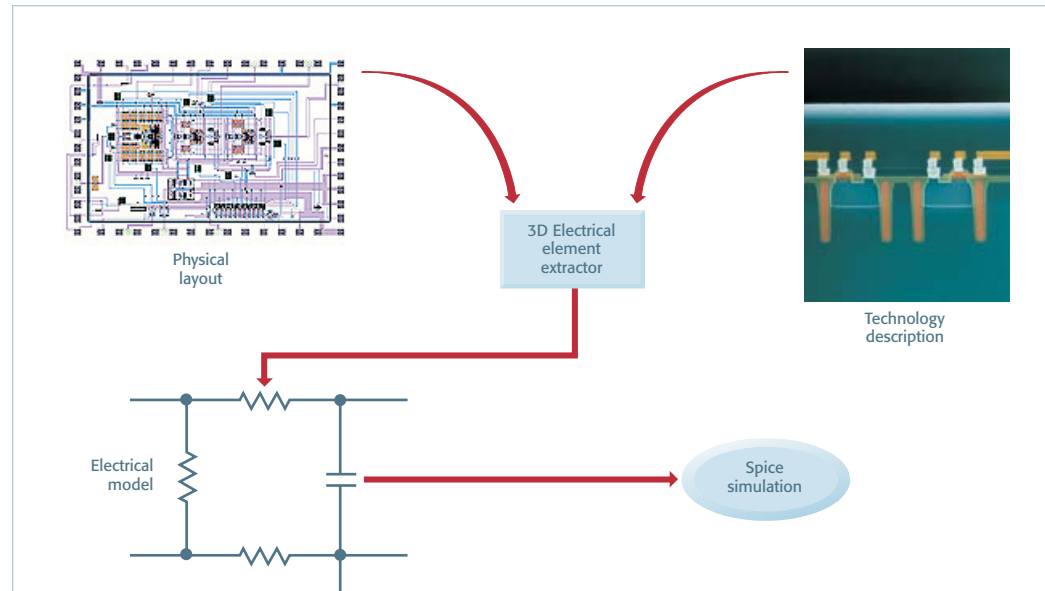
Systems' Spectre or Eldo from Mentor, they can use the noise estimates to work out if the analogue circuit needs to be protected, using guard rings, or even redesigned.

**PROCESSING TIME**

The problem with the existing methods is that they can take a long time to process, even with relatively small designs – generally extraction tools are used to analyse the aggressor circuit and produce a netlist that can be simulated in Spice. "The problem is that there is no simulator that can accommodate the sort of capacity that is needed. Companies have made lots of enhancements for model order reduction and that was OK for a certain size of analogue block. Now the problem is much much larger with SoC and SiP," said Hegazy, adding that designers have resorted to



**TODAY'S TECHNIQUES**



"Historically people have counted on different mathematical techniques to perform noise simulation," Hazem Hegazy, of Mentor Graphics, explained.

The aim, typically, is to build a network of equivalent components to the circuit above the substrate that can be

simulated in Spice. The first step is to use a three-dimensional electrical element extraction tool to build a mesh of circuit components.

The surface mesh is defined by the layout of the electrical circuit itself, with the vertical part of the mesh defined by the doping

profile of the substrate. For example, the most heavily doped part of a substrate will often be quite shallow. The doping will tail off the further you go into the substrate.

Engineers have a choice over the way in which the extraction tool works. Finite element methods give exact

solutions but they use a massive 3D matrix," said Hegazy. Finite difference methods still result in a large matrix, but it can produce a reduced RC matrix, he added.

Once the model is ready, it can be processed in a commercial Spice simulator.

manually intensive techniques to simplify the networks and speed up simulation.

"People in the analogue domain have had to do a lot of things. They would approximate the network below their sensitive nodes and put that into the simulation, using rules of thumb."

Thomas Steinecke, principal in design for electromagnetic compatibility in the microcontrollers group at Infineon Technologies and project leader of the Medea+ Parachute, said within-chip noise coupling is a focus of the project's wider research into EMC.

"For complex ICs, we need some form of model-order reduction so the complexity of the netlist is significantly reduced," said Steinecke. "The complexity of today's ICs demands simplified but accurate models."

The need to support larger designs is leading towards the development of simpler models that can be generated automatically. "The most recent is the macromodel," Hegazy claimed. "The macromodel is a model that is not that accurate. It can't be as accurate as a field

at different macro-modelling techniques. But we think it is a good way to go for solving this sort of problem for SoC. At Mentor, we are in continuous communication with the big IDMs to get something in place for the proper time. There is no single university that can handle this. You have to get feedback from the fabs and IDMs."

Clement said CWS has developed a set of tools that can generate models that execute faster than traditional techniques and which can pick up the various sources of noise across a chip. He added that the Wave Integrator tools can also work with early estimates of noise.

**EARLY ESTIMATES**

"Very early in the design flow it will help you create an estimation of the noise even if you have a limited description of the block. It will tell you where in the frequency spectrum you can expect the noise to be. It can give you the metric you need to go to the manager and say 'if you don't rethink the architecture we will never make this possible'," Clement explained.

"When you enter the physical design phase, it will help you compare different designs and protection techniques, to see which has the most effectiveness on the noise," Clement said.

Other tools are arriving for SoC noise analysis. Hegazy and colleagues have already come up with an extension for Calibre XRC that can reduce the resistive network under a given block to make it easier to simulate. And Cadence, which bought Clement's earlier noise-analysis company Snaketech, is working on techniques to improve the characterisation of cross-chip noise on SoCs. "It is definitely an area of interest for us and it is something we are already investigating," claimed Mehndiratta.

As the teams working on high-integration SoCs encounter more noise issues, you can expect other companies to come up with tools to help with planning for unwanted interference. ■

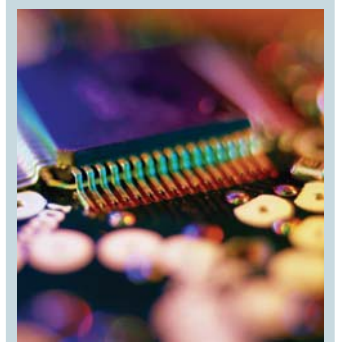
**solutions**

**FIXING THE PROBLEM**

There are not many easy fixes for noise coupling on-chip. Even those that look easy may turn out to not be that effective. For example, a guard ring looks to be a good idea for any sensitive analogue block. But it is easy to overestimate the value of the guard ring, claimed Francois Clement, chief technology officer of Coupling Wave Solutions.

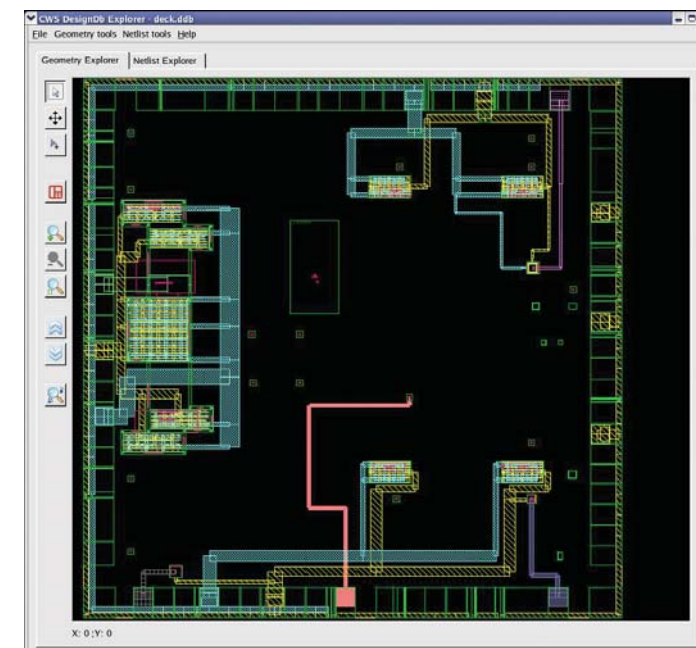
"You can't expect from guard rings that they will get rid of the noise completely, and a guard ring may need an expensive package. If you have done the design correctly, you win a maximum of 10 to 20dB noise attenuation. But when you look at the specifications of the design that you need now, this is not enough."

A guard ring may not even work at all, Clement said. "We have shown that in designs using guard rings, 80 per cent of the time, if the guard ring did not work as expected it was due to the way that the guard ring was connected."



The environment outside the chip can have an effect on how the noise is distributed within it, said Hazem Hegazy, marketing engineer at Mentor Graphics. "Below the substrate is the backplane. Usually it is grounded. But in many cases designers leave this floating. And this specific problem changes totally the model of the noise."

Hegazy said it is important that any model of noise coupling takes account of the printed circuit-board environment in which the chip is going to be introduced. A change there could render the model redundant, and turn what could have been a working device into a dud.



solver but if we can get down to a 5 per cent error, that is not too much. Researchers are now looking to have this sort of compromise: 'Let me reduce my level of accuracy to get something in place, and give me a sense of how much noise will be injected into the analogue blocks'."

Hegazy said the approach

research seems to be taking is to have a field solver produce the initial analysis of how noise will be injected into the system but then use curve-fitting functions to convert those results into simpler empirical equations. "It looks simple but is quite complex," said Hegazy.

"In my research, I am looking